Digital Electronics.

CHAPTER NINETEEN

Saturated Enhancement-Only Loaded NMOS Inverter

Introduction

In this chapter, we will describe the saturated enhancement-only loaded NMOS inverter.

The basic inverter consists of two enhancement-only NMOS transistors (size of load resistor is more one thousand larger in size than the MOSFET)

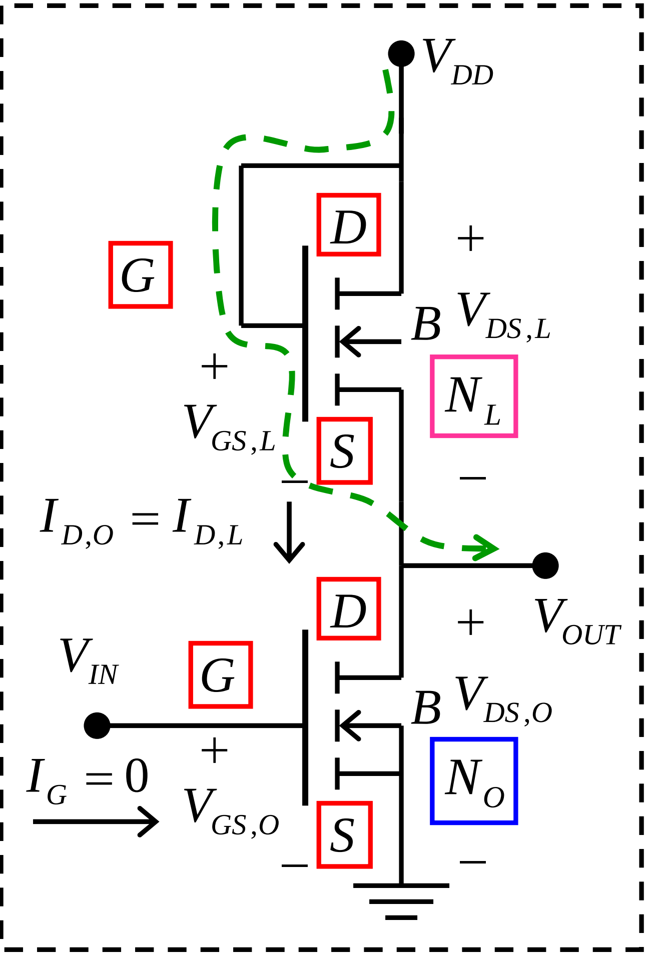
Operation of Saturated Enhancement-Only Loaded NMOS Inverter

The enhancement NMOS load device operates always in saturation

$$V_{DS,L} = V_{GS,L}$$

$$V_{DS,L}(sat) = V_{GS,L} - V_{TN,L} = V_{DS,L} - V_{TN,L}$$

$\Rightarrow$ $V_{DS,L}(sat) < V_{DS,L}$ — N_L is in saturation operation



$V_{IN} = V_{GS,O}$ $\quad$ $V_{OUT} = V_{DS,O} = V_{DD} - V_{DS,L}$

When $V_{IN}=V_{GS,O}<V_{TN,O}$: → N_O is cut-off and it does not conduct current, however N_L is still in the saturation region

$$I_{D,L} = \frac{K_n}{2}\left(V_{GS,L} - V_{TN,L}\right)^2 = 0 \Rightarrow V_{GS,L} = V_{TN,L}$$

$\Rightarrow$ $V_{OUT} = V_{DD} - V_{GS,L}$ High

Operation of Saturated Enhancement-Only Loaded NMOS Inverter

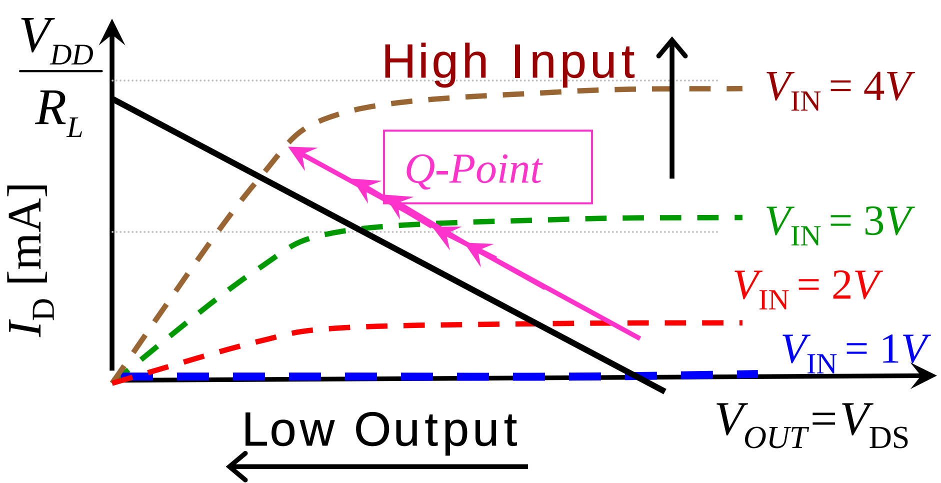
As $V_{IN}=V_{GS,O}>V_{TN,O}$:→ N_O starts to conduct (saturation), while N_L is still in the saturation region

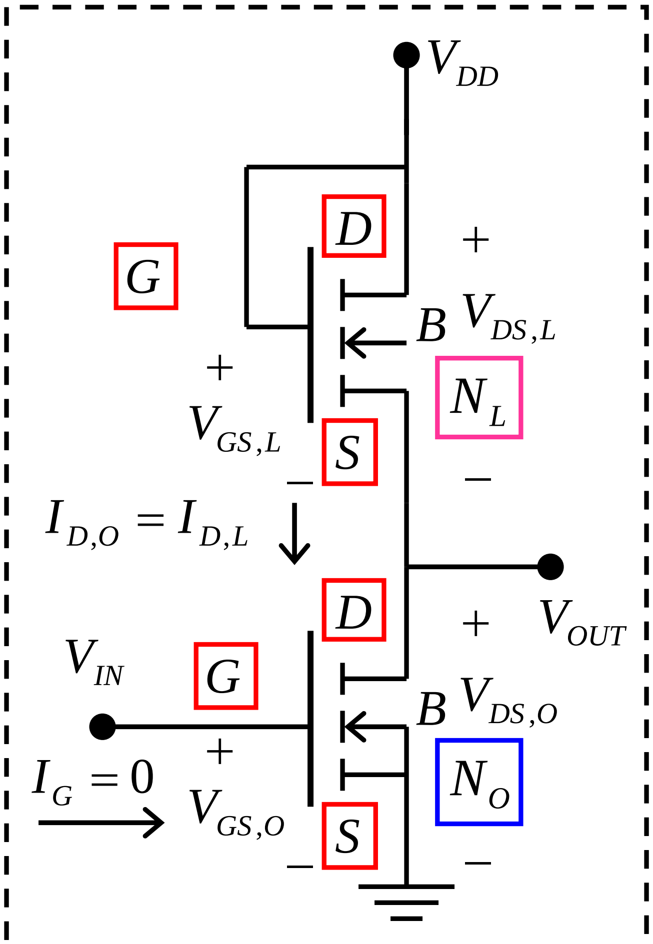
$$I_{D,O}(sat)=I_{D,L}(sat)$$

$$\frac{K_{n,O}}{2}\left(V_{GS,O}-V_{TN,O}\right)^2=\frac{K_{n,L}}{2}\left(V_{GS,L}-V_{TN,L}\right)^2$$

$$V_{IN}=V_{GS,O}$$

$$V_{GS,L}=V_{DD}-V_{OUT}$$





Operation of Saturated Enhancement-Only Loaded NMOS Inverter

As $V_{IN}=V_{GS,O}>V_{TN,O}$:→ N_O starts to conduct (saturation), while N_L is still in the saturation region

$$\frac{K_{n,O}}{2}\left(V_{GS,O}-V_{TN,O}\right)^2=\frac{K_{n,L}}{2}\left(V_{GS,L}-V_{TN,L}\right)^2$$

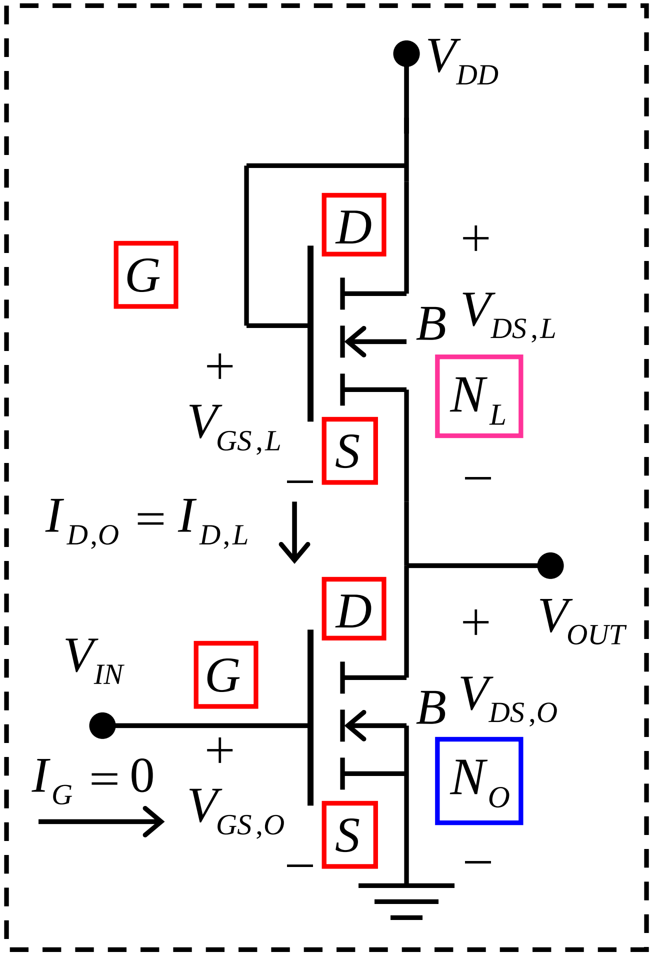
$V_{IN}=V_{GS,O}$

$V_{GS,L}=V_{DD}-V_{OUT}$

$$\sqrt{\frac{K_{n,O}}{K_{n,L}}}\left(V_{IN}-V_{TN,O}\right)=\left(V_{DD}-V_{OUT}-V_{TN,L}\right)$$

$$\sqrt{\frac{K_{n,O}}{K_{n,L}}}\left(V_{IN}-V_{TN,O}\right)=\left(V_{DD}-V_{TN,L}\right)-V_{OUT}$$

$$V_{OUT}=-\sqrt{\frac{K_{n,O}}{K_{n,L}}}V_{IN}+\sqrt{\frac{K_{n,O}}{K_{n,L}}}V_{TN,O}+\left(V_{DD}-V_{TN,L}\right)$$



Slope = $-(K_{n,O}/K_{n,L})^{1/2}$

Ch. 19

Operation of Saturated Enhancement-Only Loaded NMOS Inverter

N_O stays in saturation as long as $V_{OUT} > V_{GS,O} - V_{Tn,L}$, but if $V_{OUT} = V_{DS,O} < V_{GS,O} - V_{Tn,L}$ then *N_O* moves into linear region

$$\frac{K_{n,O}}{2}\left(2\left(V_{GS,O} - V_{TN,O}\right)V_{DS,O} - V_{DS,O}^2\right) = \frac{K_{n,L}}{2}\left(V_{GS,L} - V_{TN,L}\right)^2$$

$$V_{IN} = V_{GS,O}$$

$$V_{GS,L} = V_{DD} - V_{OUT}$$

$$\frac{K_{n,O}}{2}\left(2\left(V_{IN} - V_{TN,O}\right)V_{OUT} - V_{OUT}^2\right) = \frac{K_{n,L}}{2}\left(V_{DD} - V_{OUT} - V_{TN,L}\right)^2$$

$$2\frac{K_{n,O}}{K_{n,L}}\left(V_{IN} - V_{TN,O}\right)V_{OUT} - \frac{K_{n,O}}{K_{n,L}}V_{OUT}^2 = V_{OUT}^2 - 2\left(V_{DD} - V_{TN,L}\right)V_{OUT} + \left(V_{DD} - V_{TN,L}\right)^2$$

$$\left(1 + \frac{K_{n,O}}{K_{n,L}}\right)V_{OUT}^2 - 2\left[\left(V_{DD} - V_{TN,L}\right) + \frac{K_{n,O}}{K_{n,L}}\left(V_{IN} - V_{TN,O}\right)\right]V_{OUT} + \left(V_{DD} - V_{TN,L}\right)^2 = 0$$

Operation of Saturated Enhancement-Only Loaded NMOS Inverter

$$\left(1+\frac{K_{n,O}}{K_{n,L}}\right)V_{OUT}^{2}-2\left[\left(V_{DD}-V_{TN,L}\right)+\frac{K_{n,O}}{K_{n,L}}\left(V_{IN}-V_{TN,O}\right)\right]V_{OUT}+\left(V_{DD}-V_{TN,L}\right)^{2}=0$$

$$V_{OUT}=\frac{2\left[\left(V_{DD}-V_{TN,L}\right)+\frac{K_{n,O}}{K_{n,L}}\left(V_{IN}-V_{TN,O}\right)\right]}{2\left(1+\frac{K_{n,O}}{K_{n,L}}\right)}\pm\frac{\sqrt{4\left[\left(V_{DD}-V_{TN,L}\right)+\frac{K_{n,O}}{K_{n,L}}\left(V_{IN}-V_{TN,O}\right)\right]^{2}-8\left(1+\frac{K_{n,O}}{K_{n,L}}\right)\left(V_{DD}-V_{TN,L}\right)^{2}}}{2\left(1+\frac{K_{n,O}}{K_{n,L}}\right)}$$

EXACT SOLUTION

$$V_{OUT}=\frac{\left(V_{DD}-V_{TN,L}\right)^{2}}{2\left[\left(V_{DD}-V_{TN,L}\right)+\frac{K_{n,O}}{K_{n,L}}\left(V_{IN}-V_{TN,O}\right)\right]}$$

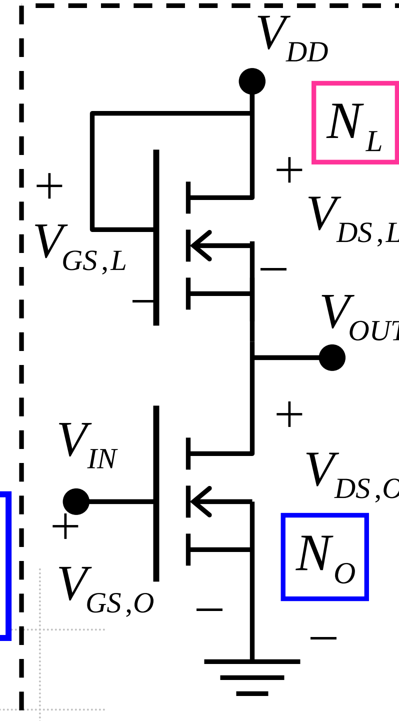
APPROXIMATED SOLUTION

VTC of Saturated Enhancement-Only Loaded NMOS Inverter

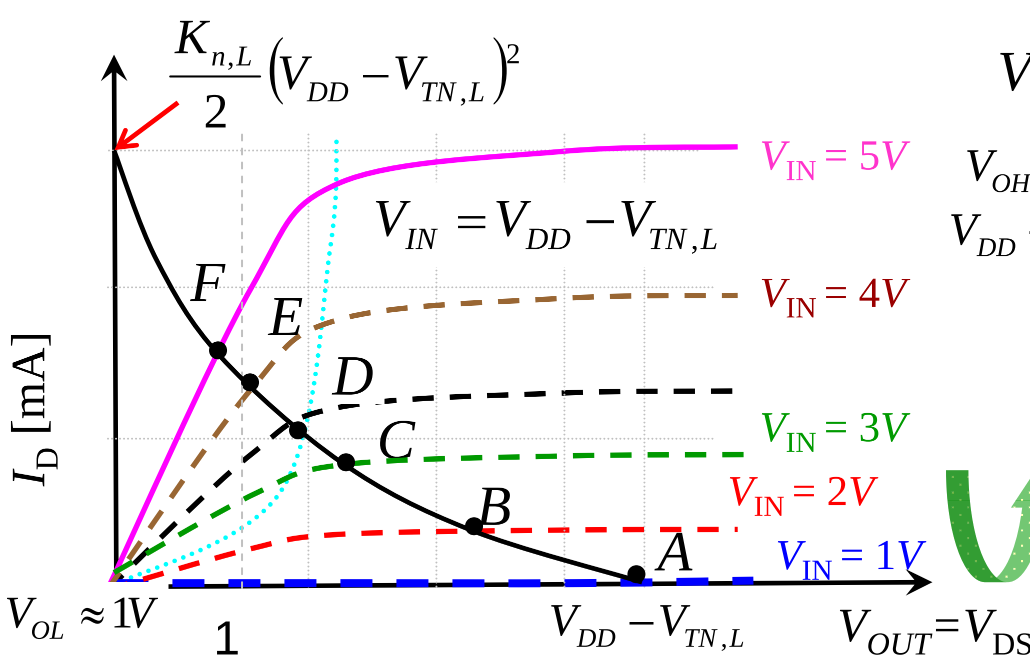
<u>Graphical determination of VTC</u> :

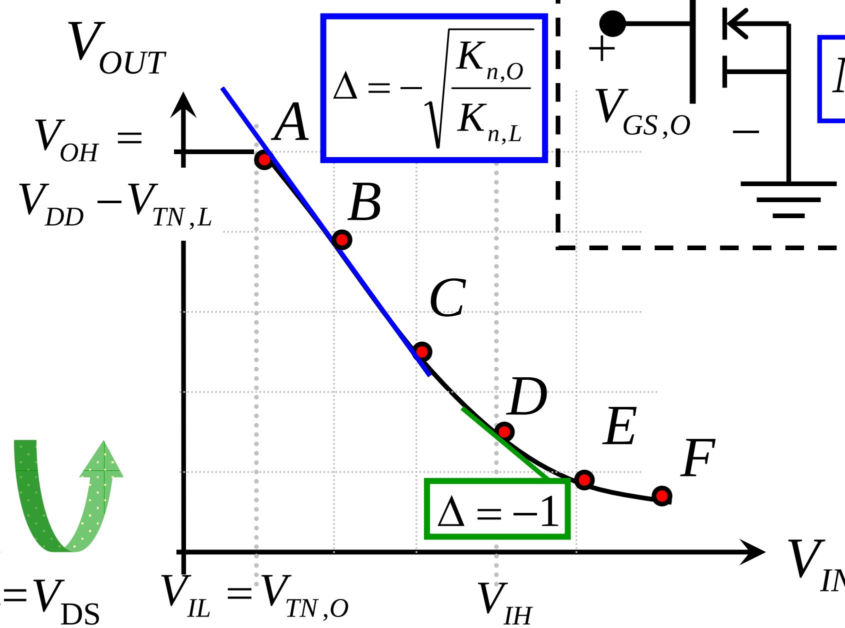
$$V_{IN} = V_{GS} \quad , \quad V_{OUT} = V_{DS}$$

Load line: $\boxed{I_{D,O} = I_{D,L} = \frac{K_{n,L}}{2}\left(V_{DD} - V_{DS,O} - V_{TN,L}\right)^2}$



From the intersections between the load line and the current-voltage characteristics, the pairs (V_{IN}, V_{OUT}) can be determined





VTC of Saturated Enhancement-Only Loaded NMOS Inverter

Analytical determination of VTC :

$\boxed{V_{OH}}$

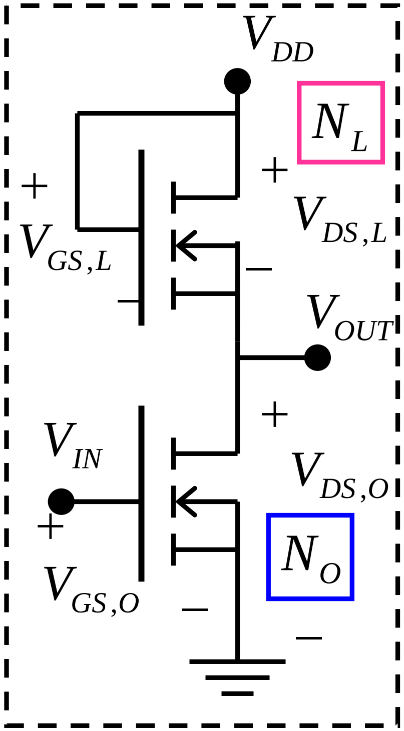
When V_{IN} is low, i.e. $V_{IN}=V_{GS}<V_{TN}$:→ N_O is cut-off

$$I_L = I_D = 0 \qquad \boxed{V_{OH} = V_{DD} - V_{TN,L}}$$

$\boxed{V_{IL}}$

V_{IL} in MOSFET is **not** defined from $dV_{OUT}/dV_{IN} = -1$

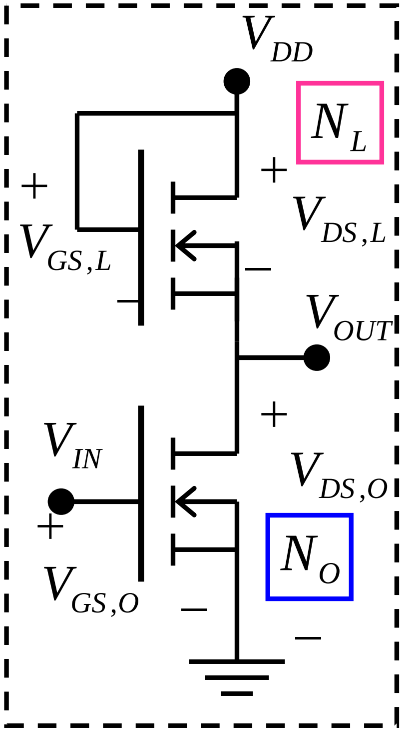
$$\boxed{V_{IL} = V_{TN,O}}$$



VTC of Saturated Enhancement-Only Loaded NMOS Inverter

Analytical determination of VTC :

$\boxed{V_{OL}}$



For the low output state, the N-MOS operates in linear mode:

$$I_D = \frac{K_n}{2}\left[2\times(V_{GS}-V_{TN})V_{DS}-V_{DS}^2\right]$$

Now, just as an assumption that the MOS is driven by a similar gate, i.e. $V_{IN}=V_{GS,O}=V_{OH}=V_{DD}-V_{TN,L}$.

$$\boxed{\frac{K_{n,O}}{2}\left(2(V_{GS,O}-V_{TN,O})V_{DS,O}-V_{DS,O}^2\right)=\frac{K_{n,L}}{2}(V_{GS,L}-V_{TN,L})^2}$$

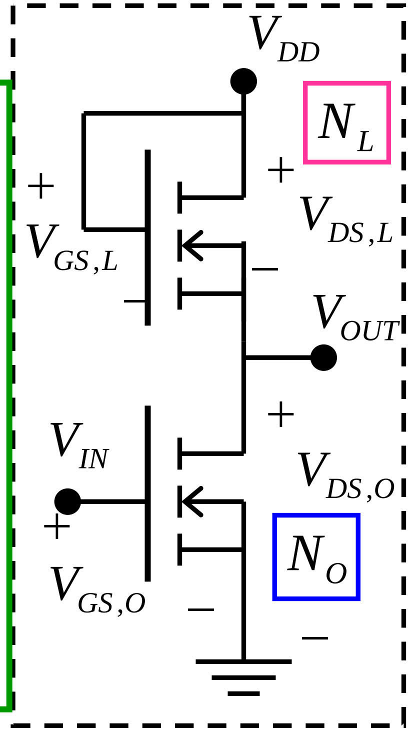
$$\boxed{\frac{K_{n,O}}{2}\left(2(V_{DD}-V_{TN,L}-V_{TN,O})V_{OL}-V_{OL}^2\right)=\frac{K_{n,L}}{2}(V_{DD}-V_{OL}-V_{TN,L})^2}$$

VTC of Saturated Enhancement-Only Loaded NMOS Inverter

Analytical determination of VTC :

$$V_{OL} = \frac{2\left[\left(V_{DD} - V_{TN,L}\right) + \frac{K_{n,O}}{K_{n,L}}\left(V_{DD} - V_{TN,L} - V_{TN,O}\right)\right]}{2\left(1 + \frac{K_{n,O}}{K_{n,L}}\right)} \pm \frac{\sqrt{4\left[\left(V_{DD} - V_{TN,L}\right) + \frac{K_{n,O}}{K_{n,L}}\left(V_{DD} - V_{TN,L} - V_{TN,O}\right)\right]^2 - 8\left(1 + \frac{K_{n,O}}{K_{n,L}}\right)\left(V_{DD} - V_{TN,L}\right)^2}}{2\left(1 + \frac{K_{n,O}}{K_{n,L}}\right)}$$

EXACT SOLUTION

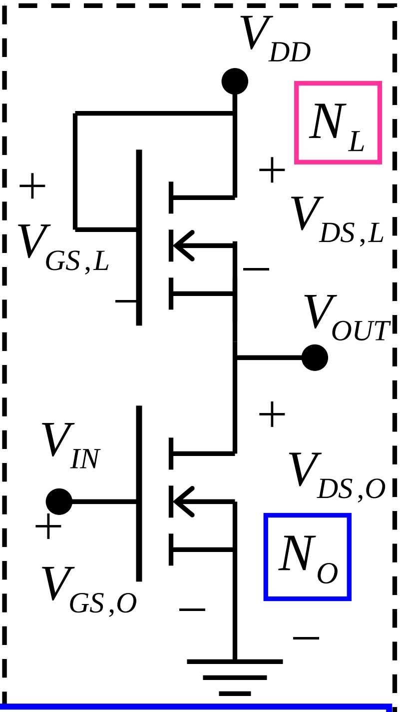


$$V_{OL} \cong \frac{\left(V_{DD} - V_{TN,L}\right)^2}{2\left[\left(V_{DD} - V_{TN,L}\right) + \frac{K_{n,O}}{K_{n,L}}\left(V_{DD} - V_{TN,L} - V_{TN,O}\right)\right]}$$

APPROXIMATED SOLUTION

VTC of Saturated Enhancement-Only Loaded NMOS Inverter

<u>Analytical determination of VTC</u> :



$\boxed{V_{IH}}$

V_{IH} in MOSFET is defined as the input voltage slightly before $V_{OUT}=V_{OL}$ where slope=-1 or

$$\frac{dV_{OUT}}{dV_{IN}} = -1$$

For high input voltages (i.e. $V_{OUT} \rightarrow V_{OL}$), N_O is in <u>linear operation</u>

$$\boxed{\frac{K_{n,O}}{2}\left(2\left(V_{IN}-V_{TN,O}\right)V_{OUT}-V_{OUT}^2\right)=\frac{K_{n,L}}{2}\left(V_{DD}-V_{OUT}-V_{TN,L}\right)^2}$$

$$\boxed{\frac{K_{n,O}}{2}\left(2\left(V_{IN}-V_{TN,O}\right)\frac{dV_{OUT}}{dV_{IN}}+2V_{OUT}-2V_{OUT}\frac{dV_{OUT}}{dV_{IN}}\right)=-K_{n,L}\left(V_{DD}-V_{OUT}-V_{TN,L}\right)\frac{dV_{OUT}}{dV_{IN}}}$$

$$\boxed{K_{n,O}\left(-\left(V_{IN}-V_{TN,O}\right)+2V_{OUT}\right)=K_{n,L}\left(V_{DD}-V_{OUT}-V_{TN,L}\right)}$$

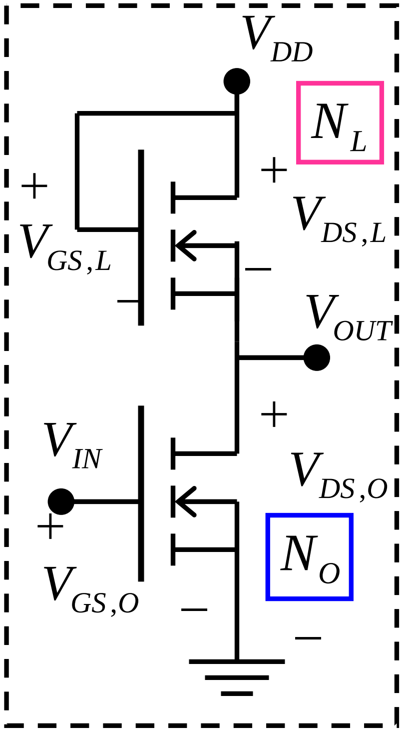
VTC of Saturated Enhancement-Only Loaded NMOS Inverter

Analytical determination of VTC :

V_{IH}

V_{IH} in MOSFET is defined as the input voltage slightly before $V_{OUT}=V_{OL}$ where slope=-1 or

$$\frac{dV_{OUT}}{dV_{IN}}=-1$$



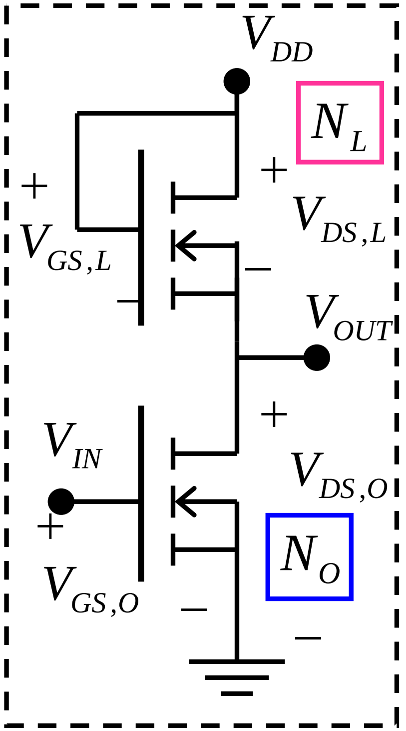
For high input voltages (i.e. $V_{OUT}\rightarrow V_{OL}$), N_O is in linear operation

$$\boxed{V_{OUT}(IH)=\frac{K_{n,O}(V_{IN}-V_{TN,O})+K_{n,L}(V_{DD}-V_{TN,L})}{2K_{n,O}+K_{n,L}}}$$

$$\boxed{V_{IH}=\frac{V_{DD}-V_{TN,L}}{\frac{1}{2}+\sqrt{\frac{3}{4}\frac{K_{n,O}}{K_{n,L}}}}+V_{TN,O}}$$

$$\text{must } V_{DS}\le(V_{GS}-V_{TN}) \quad \boxed{\text{i.e. } V_{OUT}(IH)\le(V_{IH}-V_{TN,O})}$$

VTC of Saturated Enhancement-Only Loaded NMOS Inverter



Analytical determination of VTC :

$\boxed{V_M}$ Mid point

$$V_{OUT} = V_{IN} = V_M$$

$$\Rightarrow \quad V_{DS,O} = V_{OUT} = V_M \quad \& \quad V_{GS,O} = V_{IN} = V_M$$

$$V_{DS,O}(sat) = V_{GS,O} - V_{TN,O}$$

$$= V_{DS,O} - V_{TN,O}$$

$$\Rightarrow \quad V_{DS,O}(sat) < V_{DS,O}$$

N$_O$ is in saturation operation

$$\boxed{\frac{K_{n,O}}{2}\left(V_{GS,O} - V_{TN,O}\right)^2 = \frac{K_{n,L}}{2}\left(V_{GS,L} - V_{TN,L}\right)^2}$$

$$\boxed{\frac{K_{n,O}}{2}\left(V_M - V_{TN,O}\right)^2 = \frac{K_{n,L}}{2}\left(V_{DD} - V_M - V_{TN,L}\right)^2}$$

Then solve for V_M

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Ch. 19

- HW #11:Solve Problems: 19.**1-3**,